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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,184	REBLEWSKI, FREDERIC	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7,8,11,12,14,19,20,24,30 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,8,11,12,14,19,20,24,30 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13 January 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Response mailed on December 22, 2005. Claims 1, 2, 7, 11, 14, 19, 24, 30, 32 and 34 were amended. Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 of the application are pending. This office action is made final.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on January 13, 2006, together with a list of patents. The patents have been considered.

Specification

3. The disclosure is objected to because of the following informalities:

Specification Page 3, Line 15, "The present invention includes the consitution of an emulation system" appears to be incorrect and it appears that it should be "The present invention includes the constitution of an emulation system".

Claim Objections

4. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

5. Claims 14 and 30 are objected to because of the following informalities:

Claim 14, Lines 10-11, "wherein at least some of said generation of testing stimuli are performed by on-chip data processing resources of said emulation ICs" repeat the previous lines 8-9 and should be deleted.

Claim 30, Line 6, "emulation state circuit elements" appears to be incorrect and it appears that it should be "emulated circuit elements".

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Quayle et al.** (U.S. Patent 6,694,464) in view of **Kim et al.** ("A reconfigurable multi-function computing cache architecture", ACM 2000).

8.1 **Quayle et al.** teaches method and apparatus for dynamically testing electrical interconnect. Specifically, as per claim 1, **Quayle et al.** teaches a logic board designed for circuit emulation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising

a plurality of input/output (I/O) pins (Abstract, L8-9; CL4, L27-30; CL16, L62-64);

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

a plurality of on-board data processing resources coupled to the emulation ICs (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26) to locally retrieve from the emulation ICs state data of emulated circuit elements (CL18, L5-9; CL23, L63-65), responsive to a monitor and report request received through the I/O pins (CL5, L2-4; Fig.20a, Item 238), and to locally analyze the retrieved state data to detect occurrence of one or more events, as well as report on the occurrence of the one or more events upon their detection through the I/O pins (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59);

wherein the on-board data processing resources are further employed to locally generate a plurality of testing stimuli, and locally apply the locally generated testing stimuli to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to a testing request received through the I/O pins (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least one of the emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli. **Kim et al.** teaches that at least one of the emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the logic board of **Quayle et al.** with the logic board of **Kim et al.** that included at least one of the emulation ICs comprising on-chip programmable data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli, because in the computing bandwidth limited applications, the unused portions of the cache could serve the computing needs, so the on-chip resources could be utilized more efficiently (Page 85, CL1, Para 1, L4-10); the reconfigurable module would improve the execution time of the applications with a large number of data elements by a large factor (Page 85, CL1, Para 1, 17-20); such reconfigurable cache function unit modules would improve the overall performance with low

area and time overhead (Page 85, CL2, Para 4, L3-5); and the main advantage of the reconfigurable cache is on-chip processing, which implies faster processing time and no off-chip bottlenecks and the balance/utilization of on-chip caches between storage and computation (Page 88, CL2, Para 4, L9-12).

Per claim 2: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local retrieval of state data of the emulated circuit elements (CL18, L5-9; CL23, L63-65), local analysis of the retrieved state data, and reporting of event detection (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

8.2 As per claim 3, **Quayle et al.** and **Kim et al.** teach the logic board of claim 1. **Quayle et al.** does not expressly teach that at least one of the emulation ICs comprises on-chip data processing resources to cooperate and assist the on-board data processing resources to perform the local monitoring and reporting of monitored events. **Kim et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources to cooperate and assist the on-board data processing resources to perform the local monitoring and reporting of monitored

events (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

Per claim 5: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local generation and application of stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

8.3 As per claim 7, **Quayle et al.** teaches in an emulation apparatus, a method of operation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising:

receiving by an emulation logic board, through input/output (I/O) pins of the logic board, a monitor and report request (CL5, L2-4; Fig.20a, Item 238);

in response, locally retrieving from emulation ICs of the logic board state data of emulated circuit elements of a partition of an IC design being emulated (CL18, L5-9; CL23, L63-65);

locally analyzing the retrieved state data to detect occurrence of one or more events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59); and

reporting through the I/O pin, of the logic board occurrence of the one or more events, upon detection of their occurrence (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59);

wherein the method further comprises locally generating on the logic board a plurality of testing stimuli, and applying the locally generated testing stimuli to emulation circuit elements of a respective emulation IC corresponding to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to an external testing request received by the logic board through the I/O pins of the logic board (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least some of the generation of testing stimuli are performed by on-chip programmable data processing resources of the emulation ICs. **Kim et al.** teaches that at least some of the generation of testing stimuli are performed by on-chip programmable data processing resources of the emulation ICs (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

8.4 As per claim 8, **Quayle et al.** and **Kim et al.** teach the method of claim 7. **Quayle et al.** teaches analyzing the state data to detect for the one or mare events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Quayle et al. does not expressly teach that at least some of the analysis and detection are performed by on-chip data processing resources of the emulation ICs, in lieu of retrieving the

state data from the emulation ICs. **Kim et al.** teaches that at least some of the analysis and detection are performed by on-chip data processing resources of the emulation ICs, in lieu of retrieving the state data from the emulation ICs (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

8.5 As per claim 11, **Quayle et al.** teaches a logic board designed for circuit emulation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising

a plurality of input/output (I/O) pins (Abstract, L8-9; CL4, L27-30; CL16, L62-64);

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

a plurality of on-board data processing resources coupled to the emulation ICs to locally generate a plurality of testing stimuli, and locally apply the locally generated testing stimuli to emulated circuit elements of a respective emulation IC corresponding to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to a testing request received through the I/O pins (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least one of the emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli. **Kim et al.** teaches that at least one of the emulation ICs comprises on-chip programmable data

processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

Per claim 12: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local generation and application of stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

8.6 As per claim 14, **Quayle et al.** teaches in an emulation apparatus, a method of operation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising:

receiving by a logic board, through input/output (I/O) pins of the logic board, a testing request (Fig. 19, BP clocks);

in response, locally generating on the logic board a plurality testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65); and

locally applying the locally generated testing stimuli to emulation circuit elements of an emulation IC corresponding to a partition of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Quayle et al. does not expressly teach that at least some of the generation of testing stimuli are performed by on-chip programmable data processing resources of the emulation ICs. **Kim et al.** teaches that at least some of the generation of testing stimuli are performed by on-chip programmable data processing resources of the emulation ICs (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

8.7 As per claim 19, **Quayle et al.** teaches an emulation system (Fig. 12; CL18, L26-31), comprising:

a plurality of logic boards (Fig. 12; CL18, L26-31), each having a plurality of emulation integrated circuits (IC) including reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of partitions of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13), and on-board data processing resources to locally and correspondingly generate testing stimuli, and apply the generated stimuli to the emulated circuit elements of the partitions of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to testing requests received through input/output (I/O) pins of the logic boards (Fig. 19, BP clocks); and

a workstation coupled to the logic board, including electronic design automation (EDA) software (CL23, L29-31; C26, L10-13; Fig. 20, Item 700), to provide the logic boards with the testing requests (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least one of the emulation ICs of the logic boards comprises on-chip programmable data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform the local and corresponding generation and application of testing stimuli. **Kim et al.** teaches that at least one of the emulation ICs of the logic boards comprises on-chip programmable data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform the local and corresponding generation and application of testing stimuli (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

Per claim 20: **Quayle et al.** teaches that the on-board data processing resources of each of the logic board comprise storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the local and corresponding generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

8.8 As per claim 24, **Quayle et al.** teaches in an emulation system, a method of operation (Fig. 12; CL18, L26-31), comprising:

locally and correspondingly generating testing stimuli; and locally and corresponding applying the generated testing stimuli to selected ones of the emulation circuit elements of emulation ICs corresponding to respective partitions of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Quayle et al. does not expressly teach that at least some of the performances of local and corresponding generation and application of testing stimuli are assisted by on-chip programmable data processing resources of the emulation ICs of the logic boards. **Kim et al.** teaches that at least some of the performances of local and corresponding generation and application of testing stimuli are assisted by on-chip programmable data processing resources of the emulation ICs of the logic boards (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

8.9 As per claim 30, **Quayle et al.** teaches in an emulation integrated circuit (IC), a method of operation (CL1, L24-33), comprising

detecting occurrence of one or more events; and reporting on occurrence of the one or more events upon detecting their occurrence (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Quayle et al. does not expressly teach locally retrieving on the emulation IC, using on-chip data processing resources, state data of emulated circuit elements of the emulation IC corresponding to a partition of an IC design being emulated; locally analyzing the state data of the emulation state circuit elements, using on chip data processing resources; and locally generating testing stimuli using the on-chip programmable data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using the on-chip data

processing resources. **Kim et al.** teaches locally retrieving on the emulation IC, using on-chip data processing resources, state data of emulated circuit elements of the emulation IC corresponding to a partition of an IC design being emulated; locally analyzing the state data of the emulation state circuit elements, using on chip data processing resources; and locally generating testing stimuli using the on-chip programmable data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using the on-chip data processing resources (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

8.10 As per claim 32, **Quayle et al.** teaches an emulation integrated circuit (IC) (CL1, L24-33), comprising

a plurality of reconfigurable logic and interconnect resources configured to form emulated circuit elements corresponding to a partition of an IC design being emulated (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13).

Quayle et al. does not expressly teach programmable on-chip data processing resources coupled to the reconfigurable logic and interconnect resources to locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of the emulated circuit elements. **Kim et al.** teaches programmable on-chip data processing resources coupled to the reconfigurable logic and interconnect resources to locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of the emulated circuit elements (Page 85, CL1,

Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

8.11 As per claim 33, **Quayle et al.** and **Kim et al.** teach the emulation IC of claim 32. **Quayle et al.** teaches the local generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Quayle et al. does not expressly teach that he on-chip data processing resources comprise a storage medium having stored therein programming instructions. **Kim et al.** teaches that he on-chip data processing resources comprise a storage medium having stored therein programming instructions (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

8.12 As per claim 34, **Quayle et al.** teaches in an emulation integrated circuit (IC) (CL1, L24-33), a plurality of reconfigurable logic and interconnect resources configured to form emulated circuit elements corresponding to a partition of an IC design being emulated (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13).

Quayle et al. does not expressly teach the method of operation comprising locally generating on the emulation IC testing stimuli, using programmable on-chip data processing resources; and locally applying the testing stimuli, using the programmable on-chip data

processing resources, to at least one of the emulated circuit elements. **Kim et al.** teaches the method of operation comprising locally generating on the emulation IC testing stimuli, using on-chip data processing resources; and locally applying the testing stimuli, using the on-chip data processing resources, to at least one of the emulation circuit elements (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

Response to Arguments

9. Applicant's arguments filed on December 22, 2005 have been fully considered. The arguments with respect to 103 (a) rejections of Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 are moot in view of the new ground(s) of rejection which are applied against the amended claims.

9.1 As per the applicant's argument that "the deVries et al. article teaches a "built-in self-test methodology" for testing a fabricated (physical) integrated circuit (an A/D converter IC) to identify faulty devices, not data processing resources that locally generate and apply testing stimuli to emulation circuit elements (reconfigurable logic); deVries et al. physical device testing is very different from the testing of reconfigurable logic mapped to reconfigurable logic chips; in contrast to deVries physical device testing, the test bench testing of Quayle et al. is a testing of reconfigurable logic, i.e., testing to see whether the behavior of specified logic, mapped to logic chips, meets the intended objectives; this testing occurs before any fabrication of a physical IC;

thus, one of ordinary skill in the art would not have found deVries et al.'s built-in self-test (BIST) methodology to have applicability to the logical testing of Quayle et al., and would not have found it obvious to combine the references as proposed; moreover, even if one were to make the asserted combination of Quayle et al. and deVries et al., the claimed inventions would not result; as set forth in the clarified claims presented herewith, the on-chip data processing resources of the inventions are on-chip programmable data processing resources; the specification, page 20, lines 5-8, describes that the on-chip data processing resources 1002 illustrated in Fig. 10 may execute selected ones of the software components illustrated in Fig. 4 (which include Test Stimuli Generator/Applicator 410); on the other hand, the result of the asserted combination would be an integrated circuit with fixed-function built-in self-test (BIST) circuitry.", the examiner has used a new reference **Kim et al.** against the amended claims which refer to programmable on-chip processing.

Kim et al. teaches that at least one of the emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli (Page 85, CL1, Para 1, L4-10 and L15-17; Page 85, CL2, P1, L1-2; Page 85, CL2, Para 3, L1-4; Page 85, CL2, Para 4; Page 86, CL2, Para 3, L7-9; Page 88, CL2, Para 4, L9-12).

Conclusion

ACTION IS FINAL

10. Applicant's amendment of December 22, 2005 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
February 26, 2006

Paul L. Rodriguez 3/2/06
Primary Examiner
Art Unit 2125